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Title: LANL SpaceVPX Xilinx KU060 Processor

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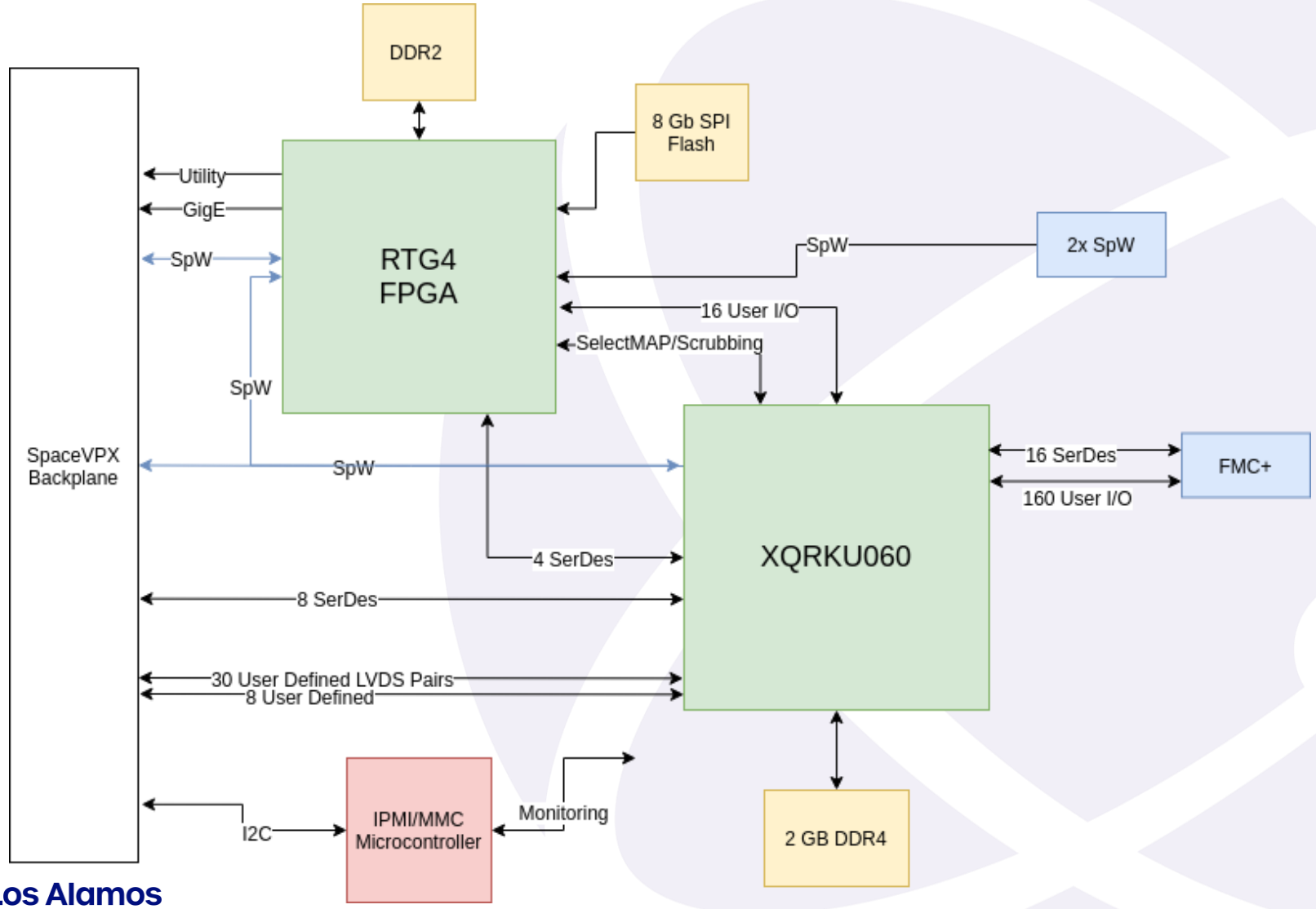
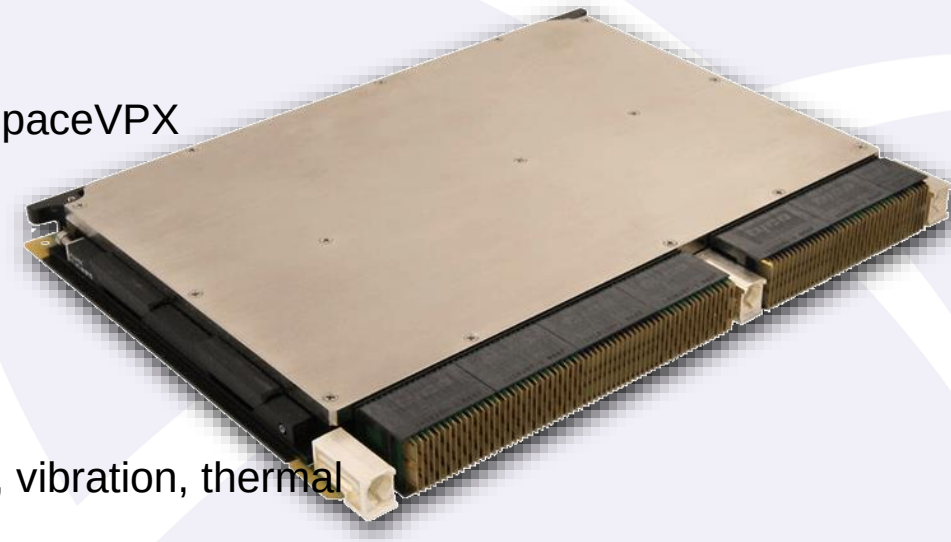
LANL SpaceVPX Xilinx KU060 Processor - Block Diagram



LANL SpaceVPX KU060 Processor - Overview

- 6U Eurocard VPX
  - 233mm x 160 mm
  - Interoperable between OpenVPX and SpaceVPX
  - Complies with ANSI/VITA 65 and 78
- For use in GEO / MEO / LEO Orbits
  - 100 Krad TID
  - Latch-up immune 103 MeV/mg/cm2
  - Mechanically Hardened
  - Meet or Exceed NASA GEVS for shock, vibration, thermal
  - Conduction Cooled Frame
  - Hypertac Connectors
  - QMLV or Class S components
- 104W available to KU060 (logic, transceivers, DDR4, IO, etc)
  - 20W available to FMC (Vadj,3.3v)
  - 43W available to RTG4 (logic, transceivers, DDR2, IO, etc)
  - Estimated 12W to boot



LANL SpaceVPX KU060 Processor – Available Resources

- FPGA Specifications

Resource	XQRKU060	RTG4
LUTs	331,680 (6LUTs)	151,824 (4LUTs)
BRAM	38,880 Kbit	5,102 Kbit
DSP48	2,760	462 (18x18 mult)
Transceivers	32 (12.5 GB/s)	24 (3.25 Gb/s)
TID	100Krad	100Krad
Ext. Memory	4 GB DDR4 (1600 MT/s x 8 bytes) ECC 12.8 GB/s – excluding parity	256 MB DDR2 (3.2GB/s) ECC; 1 GB SPI Flash (16 MB/s)
Ext. Connections	FMC+ (16 Transceivers, 80 LVDS pairs) 8 Transceivers to BP. 30 LVDS pairs to BP SpW	4 Transceivers to BP, SpW to BP (and FP) Utility IO

- Utility and SOH Microcontroller
  - UT32M0R500 – ARM Cortex M0+, 50Mhz, 96KB SRAM, 8MB Flash, ADC, DACs, I2C, SPI, UART, WDT, FreeRTOS or RTX (Keil), 50 Krad
- KU060 bitstream programming and scrubbing implemented using a soft processor in RTG4 and Xilinx Selectmap interface

Spare Slides